

# CompactPCI : A Solution for the Next Generation of Computer Telephony Integration (CTI)

## Definition

Computer telephony integration (CTI) is a term to which many are becoming accustomed. It encompasses an entire industry, devoted to the closer integration of telephony systems with computer-control devices, as well as an everexpanding range of applications. At the forefront of this industry are innovative products, built using hardware able to terminate digital telephony tier 1 (T1) and E1 (T1 European equivalent) trunk interfaces, fax and voice processing resources, voice-over-IP (VoIP) technology, and other standard peripheral devices. Typically, these operate in industrialized chassis housings and act as switches, voice-mail servers, automatic call distributors (ACDs), and nearly any other kind of telco equipment imaginable. The CTI revolution has led to a generation of such equipment, upsetting traditional notions of how telephony networks should be built.

## Overview

Over the years, various standards and specifications have been adopted to propel CTI technology. Recently, a new generation of standards emerged, at the forefront of which is CompactPCI.

CompactPCI is a new standard for computer backplane architecture and peripheral integration, defined and developed by the peripheral component interconnect (PCI) industrial computers manufacturers group (PICMG) and capable of dramatically raising the stakes in the world of computer telephony. Combining the practicalities and real-world economics of the conventional personal computer (PC) world with the kind of features long-demanded by telcos, CompactPCI sets the standard for a new generation of CTI products. For the first time, integrators can cheaply and efficiently build rugged, high-density systems with the added advantage of hot swappability.

# Topics

1. Background and Beginnings
2. A New Standard
3. The CompactPCI Backplane
4. Connectivity and Capacity
5. Secure Access: the Key to Operational Convenience
6. The Hot Swappability Revolution
7. Software, Integration, and Processes
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## 1. Background and Beginnings

Various standards have been used by manufacturers to design and develop hardware for use in computer-based products. Several manufacturers are particularly interested in peripherals that can be integrated into a given form of host processor and chassis unit, and there are a number of different means by which this can be achieved.

All have in common the principal that peripherals should be placed into a backplane, which also hosts some kind of processor. The peripherals occupy slots on the backplane, derive their power from this, and utilize the host processor to drive the applications associated with them. In this tutorial, peripherals are referred to as cards that are inserted directly into vacant slots on a backplane—in association with a host processor or central processing unit (CPU)—and housed within some kind of casing. Information from one card can be routed to another in the same system via a communications path known as a bus. This general architecture is analogous to a home computer with an incorporated sound card and modem.

In telephony systems terminating E1 or T1 physical interfaces, for example, a typical application may require that data or signals be switched from inputs to selected outputs. Such information may consist of telephone calls, for instance. Because each peripheral unit will terminate a finite number of such interfaces, larger systems can be designed by incorporating several of these cards into vacant slots on the backplane and allowing signal transfer between cards using the backplane bus. In this way, low-cost, PC-based switches that terminate large numbers of E1s or T1s can be assembled.

Backplane technology and the means by which information is routed between cards in the system (e.g., bus technology) evolved rapidly, and a number of different standards emerged. For instance, simple PC architecture using the industry standard architecture (ISA) bus allowed numerous ISA-compatible cards to be inserted into a system. However, in order to transport information across the ISA bus between cards, large numbers of so-called bus drivers and physical transceivers were required by the ISA-card software and hardware. These added cost to systems and also, unfortunately, introduced delays in signal transfer between the cards in a system. In systems where time delay is critical (i.e. telephony switches), this delay clearly had significant drawbacks.

The solution was to separate the bus between the cards from the backplane itself. Hence, new forms of communication between cards emerged, such as multivendor integration protocol (MVIP), signal computing system architecture (SCSA), and pulse code modulation expansion bus (PEB). These specifications required dedicated chipsets to generate the signals between cards and cope with the transceiver requirements. Physically, these intercard highways assumed the form of ribbon cables that connected the top edges of the cards and daisy-chained them together. This solution may allow telephony data to be switched from one card to another inexpensively, but it makes each card dependent on its peers, as no remedial action can be taken to one without dismantling the entire system.

Similarly, the physical dimensions of a PC form-factor card limit the number of terminations that can be accepted by a single card. There is a limit, therefore, on both accessibility and maximum density.

Other standards such as VersaModule Europe (VME) and MultiBus faced the same problems but resolved them with complex devices to preserve the switching interface on the backplane. However, VME has a much greater form factor than is possible within ISA systems; hence, higher-density products could be produced. VME at the simplest level is an open standard, supported by a wide range of vendors, and it became the most common bus interface on medium-sized telecommunications platforms. It offered scalability and a high degree of durability but still had many limitations.

Developers searched for a new means of ensuring intercard communications, while maximizing system density, interoperability, and reliability. High-end systems, produced by the principal switch vendors, necessarily utilized proprietary interfaces to achieve these goals. While newer technologies lacked key features such as interoperability, they would always be considered poor relations in the demanding telco environment, where five-9 reliability is often considered the norm.

Recently, an entirely new standard emerged that addresses all of these issues and may be the catalyst required to confer global acceptability to the computer-telephony industry: CompactPCI.

## 2. A New Standard

CompactPCI and PCI technologies have emerged from the search for a standard interface between peripherals on PC-compatible CPUs and backplanes. In keeping with the requirements for true interoperability, the PICMG, which is an independent and cooperative consortium of vendors and manufacturers, has overseen the development of these specifications.

The PICMG is primarily focused on the evolution and development of specifications for PCI and CompactPCI products, and the diversity of membership ensures that all interested parties can be represented and that interoperability can be maintained to produce a common specification, accessible to all.

PICMG specifications define hardware practices. Software communication and bus architecture, however, have been defined by a second independent interest group, the Enterprise Computer Telephony Forum (ECTF). The ECTF was founded to converge the plethora of competing standards for computer telephony (CT) buses and to improve interoperability between manufacturers. Essential to this process is introducing better notions of scalability, so that solutions can be built to serve the needs of different environments while utilizing the same core technology. To this end, the ECTF has produced two specifications for hardware and software bus interfaces: H.100 and H.110, also known as CT buses. The two organizations work in tandem to develop all aspects of the CompactPCI standard.

## 3. The CompactPCI Backplane

As indicated, the backplane is crucial to any scalable system. CompactPCI defines a new backplane technology that confers a number of key benefits to manufacturers. These benefits are based upon the combination of three key factors:

- PCI silicon support
- 2-mm standard personal identification number (PIN) connectors
- large form factor

The PCI standard is a bus standard developed for PCs by Intel that can transfer data between the CPU and card peripherals at much faster rates than are possible via the ISA bus (e.g., about 132 Mbps as opposed to 5 Mbps). PCI was originally designed for standardizing the interfaces available on chips to be used on PC-compatible peripherals and was unique in that it utilized silicon. Importantly, PCI was designed with limitations to the maximum capacity of the bus and to the

electrical loading it would require. These considerations helped minimize the costs of the bus interface.

PCI was rapidly adopted by other vendors and became the most common bus interface for such chips. Despite becoming the established interface, offering high-speed data transfer, PCI lacked the higher density available from systems utilizing VME, as only four cards could be supported within a system. CompactPCI was a solution to this set of problems, given that it adopted the proven European form factor successfully utilized in VME systems.

CompactPCI uses a vertically mounted backplane consisting of five connectors, as is defined in the PICMG's CompactPCI specification 2.0. This method of mounting is significantly more robust than that available from a standard PC and also provides better access for cooling because air can flow past more easily. Telecommunications applications often require the use of large amounts of digital signal processors (DSPs), which are usually heat intensive; thus, cooling is essential.

Cards are inserted into the physical bus interface from the front of the unit, enabling straightforward access. Furthermore, the vertically orientated bus provides the possibility of access from two sides. This point is highly significant, as is explored in *Topic 4*. All in all, a CompactPCI chassis offers a rugged, secure, and highly reliable platform in which to insert communications cards for demanding applications.

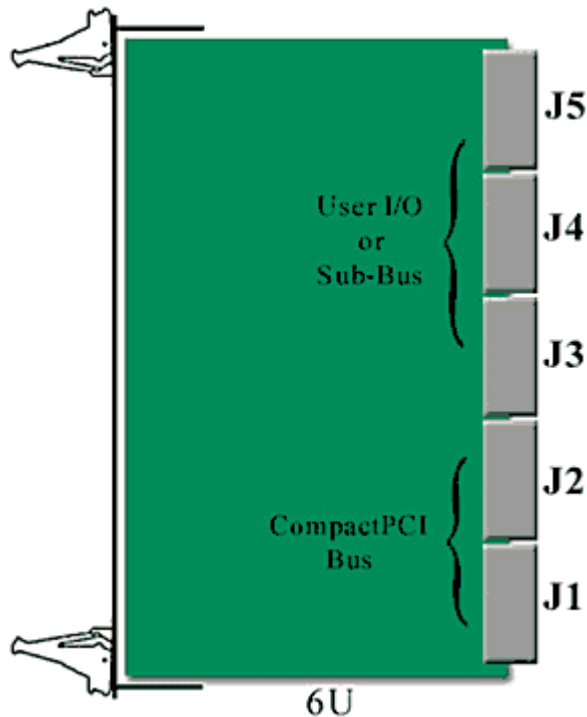
## 4. Connectivity and Capacity

CompactPCI cards can come in two different sizes (3U or 6U), but the standard defines a common physical design. There are a number of physical connectors utilized to support integration to the physical bus itself. Although different connectors are used in each version due to size discrepancies, each connector serves a specific purpose and contains a specific number of 2-mm pins (535 in all). The standard for pin connectivity was originally developed by Siemens and confers several advantages:

- power and grounding access
- high signal integrity
- minimal noise loss
- minimal noise susceptibility

This rigid definition is in contrast with the multiplicity of arrangements that have existed in previous systems and further assists the interoperability of the standard (see *Figure 1*).

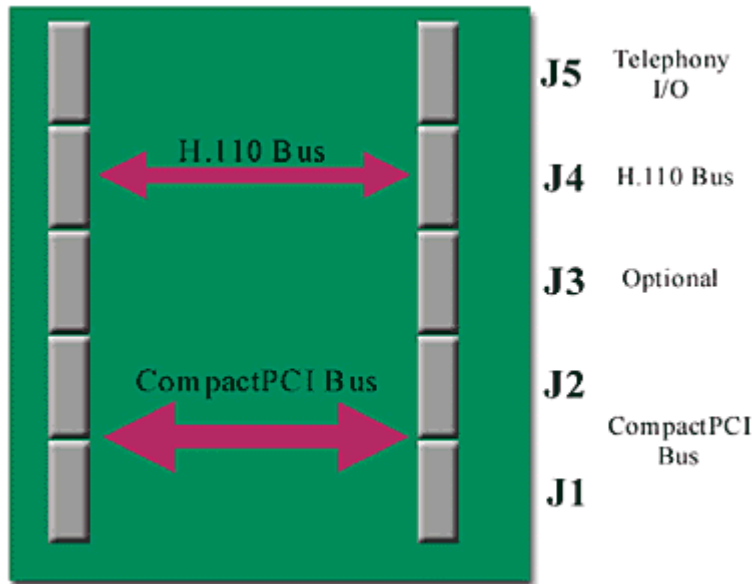
Figure 1. Rigid Definition



There are five connectors in total. J1 always acts as the 32-bit PCI bus interface. This is used by both the 3U and 6U board versions. J3, J4, and J5 are allocated for input and output signal distribution and, amongst them, offer a total of 315 2-mm connector pins. They are not present on 3U-card varieties. J2 offers an additional 32-bit bus interface as an option. Hence, when it is utilized, a total bus of 64-bits is available. Taken together, J1 and J2 constitute the CompactPCI bus and J3, J4, and J5 constitute the local or subbus. The subbus may itself be broken down, given that J4 specifically provides access to the H.110 bus, while J5 provides access to other external input and output signals. J5 will be explored in more detail in subsequent sections.

This subbus enables multiple boards to communicate with each other quickly and efficiently. In telephony applications, this is particularly important, as it allows rapid transfer of data between cards in a system. Furthermore, the simplicity of design is in contrast to the complexity of ISA or VME systems (see *Figure 2*).

Figure 2. Simplicity of Design



In addition to the allocation of connectors to the computer telephony and CompactPCI buses, specifications also require the addition of mezzanine-type daughter boards to individual CompactPCI cards. This allows CompactPCI cards to support higher processor or chip density to host DSP chips for advanced telephony applications.

Associated with the connector design, the Institute of Electrical and Electronic Engineers (IEEE) specification 1101.11, known as rear panel-transition module, has been incorporated into the CompactPCI standard. This standard requires permanent or semipermanent connectivity of inputs and outputs and gives mechanical definition to the strong grounding and shielding practices of electrical components. This is particularly important when one considers the demanding electromagnetic capability (EMC) and safety legislation now enforced by governments around the world.

The CompactPCI specification also provides a mechanism that identifies the physical position of each card and maps it into software. Thus, any one card has knowledge of the inputs and outputs, internal and physical, to which it is connected (assuming that the software is correct). Specification 1101.11 also permits specific slots to be assigned to specific cards, should this be a requirement.

At present, the physical capacity of the CompactPCI bus is limited. It can support up to eight cards, which, if one is designated the CPU, leaves seven slots free for peripheral cards. Because CompactPCI's tremendous potential for telecommunications applications was soon recognized, a standard that specifically defines how CompactPCI systems should use the H.110 bus was

originated. Known as the computer telephony specification or PICMG 2.5, it complements other CompactPCI specifications. Theoretically, this standard enables up to sixteen E1 or T1 PCMs to be terminated on a single CompactPCI card. It also suggests that up to twenty slots could be available in a single chassis, which would have the net result of allowing 320 E1 or T1s to be switched in a single unit. The largest ISA-based systems could only support thirty-two E1 or T1 terminations in a single chassis.

Although such a scenario is not presently possible, it does serve as an indication of the tremendous potential of CompactPCI to permit the design of high-density applications at low cost. However, work is underway in providing physical bridges between each CompactPCI cluster of eight cards. Such systems would combine multiple clusters in a single chassis.

A final consideration for capacity is the switching bandwidth of the H.110 CT bus itself. This has a maximum capacity of 4096 bidirectional timeslots, each with a capacity of 64 kbps. In other words, 2048 duplex call paths may be established across a single H.110 bus. This bus acts a time-division multiplexer (TDM) by supporting the transmission of various kinds of signals over the same transmission medium.

It is clear that CompactPCI offers a switching solution of great power. How that power can be realized is the subject of *Topic 5*.

## 5. Secure Access: The Key to Operational Convenience

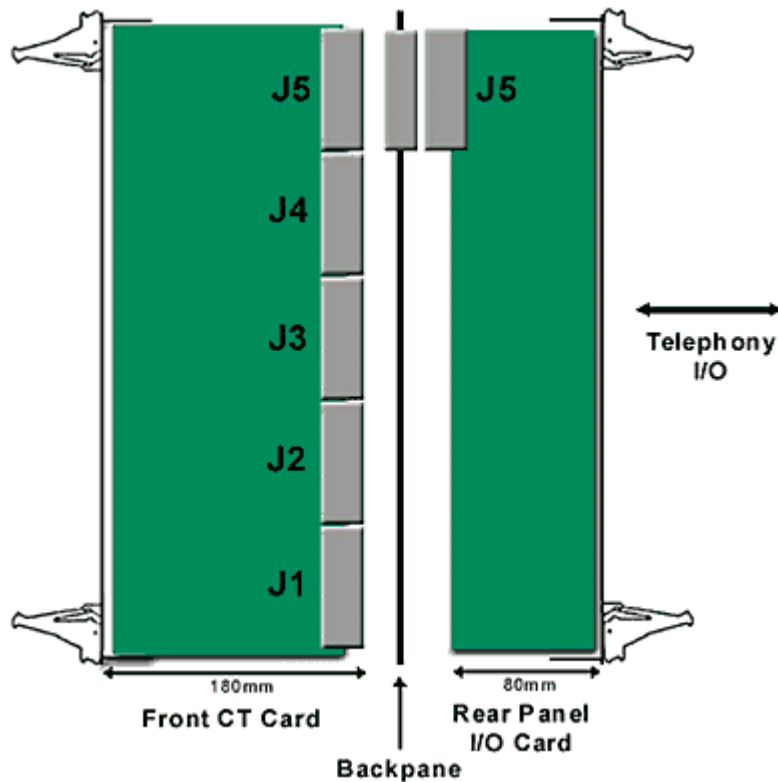
All telecommunications equipment must be physically connected to the network at some point. In an E1 or T1 switch, this means that every single E1 or T1 PCM trunk interface must plug into the appropriate termination point on the switch system. As PCM density grows, so does the tangle of cables. Clearly, to maintain operational effectiveness, a simple means of combining high levels of connectivity with ease of access to the card must be found. This is particularly important when one considers the operational implications of truly hot-swappable systems. The work of the PICMG has led to an elegant solution to this problem.

As indicated earlier, it is possible to connect a second board into the reverse of the vertically orientated CompactPCI bus interface. This permits manufacturers to design boards that serve only to terminate external input and output interfaces. All processor activity may be concentrated on the front-panel portion of the card, allowing all cabling associated with a particular card to be plugged into an electrical interface at the rear of the system. Because it is divided into two sections, the front or processor section—when it must be replaced—can simply be removed using the physical ejector levers provided without disturbing the cabling

secured to the rear portion. Technically, the rear card is known as a break-out or transition board.

The transition board is connected to the front-panel card via a mirror image of the connection interface utilized by the front card. All of the input and output interfaces for a particular rear or front combination are presented through the J5 connector pair of each, which passes across the CompactPCI backplane (see *Figure 3*).

Figure 3. Transition Board



The elegance of this system is underlined by the fact that, once again, interoperability is assured, for the IEEE 1101.11 specification defines the characteristics of the rear input and output transition card and indicates that this card should connect to that of the front panel. The transition card has a maximum depth of 80 mm, which ensures that the depth of a CompactPCI system will not exceed 300 mm. CompactPCI systems may thus be used in space-sensitive environments, particularly as they retain the small footprint that made 19-inch, rack-mounted PC systems so popular.

## 6. The Hot Swappability Revolution

One of the principal innovations of the CompactPCI standard is its introduction of hot swappability (hot swap) to CTI products. This, combined with effective simplicity and interoperability, explains the widespread appeal of the technology.

Up until this point in time, hot swap has been an asset demanded by telcos that simply could not be delivered by suppliers of PC-based CTI solutions. Available on VME in a complex implementation and not to an open standard, previous solutions have been costly and manufacturer specific. It was believed that the barrier between hot-swap and PC-based CTI solutions was unbridgeable. Now, however, CompactPCI allows true fault tolerance and security to be achieved through low cost, manageable solutions.

All large, central office (CO)-type switches are expected to have hot swappability to permit the kind of fault-tolerant architecture and reliability the telecommunications industry demands. At a stroke, CTI applications gain long-denied credibility throughout the industry.

Hot swappability or live insertion is defined as the ability to insert or remove a process card from a live system. This process places several requirements on the developer. Firstly, the procedure must be safe; a live system is, by definition, one that requires power to run an application process. Secondly, the removal or insertion of a card into the system must not cause any disruption to the ongoing processes of the application, such as switch failure. Thirdly, taking the card in and out of the system must not itself be affected by this action. Although the requirements are straightforward, they have been impossible to achieve using standard PC architectures. How, then, does CompactPCI resolve this problem?

In fact, the hot-swap standard generated by PICMG known as PICMG 2.1, announced in July 1998, is relatively simple and defines a manual procedure by which hot swap can be achieved. The procedure involves hardware and software processes linked to electrical signals and can be implemented by all manufacturers, provided that they follow the appropriate guidelines.

The procedure is dependent on several key factors. First, the silicon chips utilized by the PCI-bus architecture must be able to communicate directly with each other, not via the mediation of hardware buffers. The chips achieve a state in which their signals can be synchronized with those of the backplane. Because nothing exists between the two, synchronization may occur quickly, although the lack of mediation buffers means that the electrical loading of the bus must be precisely monitored to maintain a synchronous state.

Second, the pin connectors between the CompactPCI card and the mating contacts on the CompactPCI bus are designed to be of variable length. Given this situation, certain pins will make contact with their respective mate before others

do or, conversely, lose contact before others do so. Finally, each card is secured in place via a lever that clips into position at the front or rear of the chassis unit.

The procedure essentially follows a predictable sequence. When a card is selected for extraction, the lever is raised or released. This action breaks a contact on some associated circuitry and sends a signal to the controlling software, which, in turn, signals that a particular card is being prepared for extraction. Hence, the system can redirect processes elsewhere. Once the withdrawal process begins, certain pins will lose contact with their mates before others. In fact, there are three lengths defined by the standard. The shortest will obviously lose contact first, which sends a signal to the control system indicating that the card is being removed. Thus, power-down procedures can be initiated.

When a card is being inserted, the longest pins make contact first, thereby generating a signal that instructs the system to begin delivering power to the card. As the shortest make contact, further signals are generated that inform the system that the board is now fully in place and that all of the power-up procedures can be completed. The medium-length pins make contact as the initial charges are being applied to the card, and the PCI chip resumes operation. Closure of the security lever completes the process.

The PICMG specification defines the signals associated with each event that developers use to build hot swappability into their applications. This activity demands close monitoring at a high level to ensure that any applications in service take all necessary actions to divert resources away from the removed card or to allocate resources to an inserted card. Thus, developers must be extremely diligent.

A further consideration involves timing. All telecommunications systems are either synchronized to an external clock source or generate a clock source that must be distributed to other equipment via the telecommunications network. Telecommunications equipment does not usually accommodate several clock sources. If the card to be removed is the card that is responsible for distributing the timing signal across the system, synchronization may be lost, causing the system to run free. However, the CompactPCI bus enables the reception of two timing signals. Hence, if one source is lost, a secondary source can be provided to ensure that the system remains appropriately synchronized.

In mission-critical systems such as those experienced in the telecommunications industry, such capabilities have great importance, and their availability in such systems will undoubtedly prove to be revolutionary.

## 7. Software, Integration, and Processes

The CompactPCI backplane acts as a seamless connection between all peripherals attached to it. The CPU and all other PCI-compatible chips appear as resources

common to the entire system, while peripheral chips appear to system software as though they are co-located with chips on the CPU of a standard PC. This situation has several implications.

First, it means that no barrier exists to running software and processes that have evolved in the desktop world on CompactPCI systems; software can readily be ported from one platform to another, which represents an essential savings in time and money.

Second, provided a peripheral is CompactPCI compliant, it can be integrated into a CompactPCI platform. Integrators can simply choose devices from a vast array of vendors and plug them into their systems. In telecommunications applications, a wide variety of interfaces can be supported on the same platform, as they simply become resources within the same system and peripherals to the CompactPCI bus.

A further benefit is the fact that a wide range of operating systems can be supported within a CompactPCI system. Most operating systems that run on a PC will run on CompactPCI systems without further modification. Furthermore, developers can select the processor they require based on preference alone. This wide range of compatibility makes it a relatively straightforward task for developers to build CompactPCI systems or to transfer from one technology to another. It also confers a degree of future proofing to system design. Because all system components are peripherals of the CompactPCI bus, individual components may readily be replaced without causing disruption to the system as a whole.

Given the capabilities of this new technology, it is useful to review the applications to which it can be directed. As previously indicated, PC-based systems built around various kinds of network interfaces (e.g., E1, T1, asynchronous transfer mode [ATM], and IP) are already common. Despite their ever-growing sophistication, reliability, and cost effectiveness, such systems have not always been validated by certain sections of the industry. Conversely, other parties have cheerfully accepted the limitations of such systems. Developers have been positioned somewhere in between, trying to reconcile the demands of each community—on the one hand for cost-effective functionality and on the other for telco-grade reliability.

There is no doubt that PC solutions have answered many of the arguments against them, but objections will still be raised in some quarters. However, CompactPCI changes all of this. It offers the best of both worlds (i.e., the opportunity to develop complex systems in a cost-effective manner while addressing the issues of reliability that are raised against the PC world).

Developers have a tremendous opportunity to offer telco-grade equipment using technologies that have evolved from PCs. Rugged, fault-tolerant, reliable, and

high-density applications can readily be implemented. CompactPCI may be anticipated in all areas of the telecommunications network, and as more and more networks are rolled out by more and more operators, cost considerations will surely force purchasers in the direction of systems designed using this new technology.

The first system to offer hot swap as a truly open standard, CompactPCI is indeed revolutionary.

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## Self-Test

1. What is a bus?
  - a. a mode of transport
  - b. a vehicle
  - c. a means of communication between peripherals
  
2. Which of the following is not an intercard bus?
  - a. MVIP
  - b. SBSC
  - c. PEB
  
3. Which organization is responsible for originating hardware standards for CompactPCI?
  - a. PCIMG
  - b. PCMGI
  - c. PICMG
  
4. Which organization is responsible for defining software bus architectures for CompactPCI?
  - a. ECGF
  - b. ENTF
  - c. ECTF
  
5. What is the bandwidth of the ISA bus?
  - a. 15 Mbps
  - b. 10 Mbps
  - c. 5 Mbps

6. What is the bandwidth of the PCI bus?
  - a. 142 Mbps
  - b. 132 Mbps
  - c. 122 Mbps
7. How many connectors are there on a 6U CompactPCI card?
  - a. 2
  - b. 5
  - c. 6
8. Which connector acts as the PCI bus interface?
  - a. J1
  - b. J2
  - c. J3
9. Which connector acts as the H.110 bus interface?
  - a. J2
  - b. J3
  - c. J4
10. How many cards can a standard CompactPCI bus support?
  - a. 6
  - b. 7
  - c. 8
11. How many cards can be supported on the largest single-chassis ISA systems?
  - a. 28
  - b. 30
  - c. 32

12. Which connector is used as the interface between the front and rear modules of a CompactPCI card?
- a. J3
  - b. J4
  - c. J5
13. A compactPCI chassis has a physical footprint of \_\_\_\_\_ inches.
- a. 19
  - b. 22
  - c. 25
14. Hot swap works because of which of the following?
- a. the connector pins of the CompactPCI cards are of different lengths
  - b. the cards are robust
  - c. the cards are the right size

## Correct Answers

1. What is a bus?
- a. a mode of transport
  - b. a vehicle
  - c. a means of communication between peripherals**
- See Topic 1.
2. Which of the following is not an intercard bus?
- a. MVIP
  - b. SBSC**
  - c. PEB
- See Topic 1.

3. Which organization is responsible for originating hardware standards for CompactPCI?
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  - c. PICMG**See Topic 2.
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  - b. 5**
  - c. 6

See Topic 4.

8. Which connector acts as the PCI bus interface?

a. **J1**

b. J2

c. J3

See Topic 4.

9. Which connector acts as the H.110 bus interface?

a. J2

b. J3

c. **J4**

See Topic 4.

10. How many cards can a standard CompactPCI bus support?

a. 6

b. 7

c. **8**

See Topic 4.

11. How many cards can be supported on the largest single-chassis ISA systems?

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See Topic 5.

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a. 19

b. 22

**c. 25**

See Topic 5.

14. Hot swap works because of which of the following?

**a. the connector pins of the CompactPCI cards are of different lengths**

b. the cards are robust

c. the cards are the right size

See Topic 6.

## Glossary

### **ACD**

automatic call distributor

### **ATM**

asynchronous transfer mode

### **CPU**

central processing unit

### **CT**

computer telephony

### **CTI**

computer telephony integration

### **DSP**

digital signal processor

### **ECTF**

enterprise computer telephony forum

**EMC**

electromagnetic capability

**IEEE**

institute of electrical and electronic engineers

**ISA**

industry standard architecture

**MVIP**

multivendor integration protocol

**PCI**

peripheral component interconnect

**PCM**

pulse code modulation

**PEB**

PCM expansion bus

**PICMG**

PCI industrial computers manufacturers group

**SCSA**

signal computing system architecture

**TMC**

time-division multiplexer

**VME**

VersaModule Europe

**VOIP**

voice over Internet protocol